CLAIMS:

1. A semiconductor device comprising a semiconductor device body encapsulated in an envelope of synthetic resin material, wherein an insulating layer is present at one surface of the body, a pattern of conductive connections is present on the insulating layer and at windows in the insulating layer, an over-layer of insulating material is present on the pattern of conductive connections, and a layer pattern of ductile metal covers at least most of the surface area of the over-layer of insulating material to provide an interface with the synthetic resin material that reduces stress between the insulating material and the synthetic resin material during thermal cycling of the device, and wherein the ductile metal layer pattern comprises distinct parts that are electrically isolated and spaced from each other on the over-layer, the ductile metal is sufficiently ductile as to deform laterally on the over-layer during thermal cycling of the device, and the spacing of the electrically-isolated parts is sufficient to avoid a short circuit between the electrically-isolated parts as a result of the lateral deformation.

2. A device as claimed in Claim 1, wherein the spacing of the electrically-isolated parts of the ductile metal layer pattern is at least 15 micrometres in the device before thermal cycling.

3. A device as claimed in Claim 1 or Claim 2, wherein the device body comprises integrated circuitry, and at least one of the electrically-isolated parts of the ductile metal layer pattern extends over the over-layer over conductive connections of the integrated circuitry.

4. A device as claimed in any one of Claims 1 to 3, wherein the device body comprises integrated circuitry that includes a capacitor, a window is present in the over-layer at the area of the capacitor where a part of the pattern of conductive connections forms an upper plate of the capacitor, and at

least one of the electrically-isolated parts of the ductile metal layer pattern extends on the upper plate of the capacitor at the window in the over-layer.

5. A device as claimed in any one of Claims 1 to 4, wherein a number of the electrically-isolated parts of the ductile metal layer pattern form metal bond pads that are connected to the conductive connections at windows in the over-layer, and terminal conductors of the device are connected to the metal bond pads.

6. A device as claimed in any one of the preceding Claims, wherein at least one part of the ductile metal layer pattern is connected to the same potential as an underlying conductive area.

7. A device as claimed in Claim 6, wherein distincts parts of the ductile metal layer pattern that are electrically isolated from each other are individually connected to respective underlying conductive areas.

8. A device as claimed in Claim 7, wherein the device body comprises a power-dissipating portion and an integrated circuit portion, a part of the ductile metal layer pattern overlies the power-dissipating portion and is connected to an underlying conductive area of the power-dissipating portion, and at least one other part of the ductile metal layer pattern overlies the integrated circuit portion and is connected to an underlying conductive area of the integrated circuit portion.

9. A device as claimed in any one of the preceding Claims, wherein the device body comprises a perimeter termination structure in the vicinity of the periphery of the device body, and a part of the ductile metal layer pattern extends over the termination structure while being spaced from the periphery of the device body.

10. A device as claimed in Claim 9, wherein a part of the pattern of conductive connections extends between the termination scheme and the overlying part of the ductile metal layer pattern to screen electrically the termination scheme from the overlying part of the ductile metal layer pattern.

11. A device as claimed in any one of the preceding Claims, wherein the ductile metal layer pattern covers at least 90% of the surface area of the over-layer of insulating material.

12. A device as claimed in any one of the preceding Claims, wherein the ductile metal layer pattern has a thickness of at least 2.5 micrometres.

13. A device as claimed in any one of the preceding Claims, wherein the ductile metal layer is aluminium or an aluminium alloy.